

The Stretch® S5620 software-configurable processor, based on Stretch's revolutionary S5 engine, dramatically boosts system performance by off-loading compute-intensive tasks from a general purpose processor. By tailoring embedded programmable logic within the processor engine to the application, system developers optimize the application software and the instruction-set architecture simultaneously. Integrating high-performance I/Os at industry leading speeds, the S5620 offers remarkable performance enhancements to systems using PowerPC-based processors.

Key Features

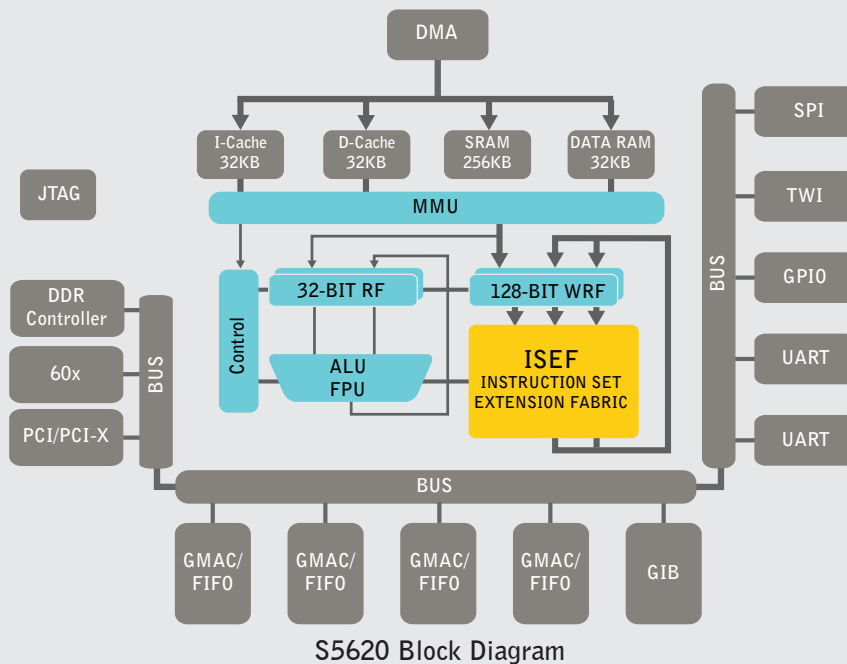
- High-performance RISC Processor Core
 - > 300 MHz, 32-bit Xtensa core
 - 16- and 24-bit instructions
 - Supports MMU with TLB
 - Single-precision floating point operations
- Stretch Instruction-Set Extension Fabric (ISEF)
 - > Aligned load and store
 - 8, 16, 32, 64, and 128 bit
 - > Unaligned load and store
 - Up to 16 bytes variable byte streaming I/O
 - Up to 32 bits variable bit streaming I/O
 - > User-defined extensions to the core ISA
- Defined in C/C++
 - Fully pipelined and interlocked
- Memory
 - > 256KB SRAM
 - > 32KB Data RAM
 - > 32KB Data Cache
 - > 32KB Instruction Cache
- Peripherals
 - > 200 MHz 60x bus for inter-processor connectivity
 - > One 64-bit DDR400 SDRAM port with ECC
 - > One 32/64-bit, PCI (66MHz) port or 133 MHz PCI-X port
 - > Four programmable parallel ports
 - 10/100/1000 Media Access Controller with MII/GMII support
 - FIFO mode (bypassing MAC)
 - > One Generic Interface Bus (GIB)
 - > Two programmable serial ports
 - Two-wire and SPI devices
 - > Two UART ports with IrDA
 - > General Purpose I/O (GPIO) and Interrupt pins
 - > One standard test port supporting JTAG IEEE 1149.1
- OS Support
 - > Support for standard operating systems
 - > Support for a coprocessor mode without OS

STRETCH ADVANTAGES

- > Dramatically boosts system performance in compute-intensive applications by customizing the S5620 ISA through the embedded programmable logic within the processor engine
- > Enables fast time-to performance
- > Reduces development and system costs
- > Provides high-performance I/Os at industry leading speeds

APPLICATIONS

- > Networking
- > Office Automation
- > Video and Imaging



S5620 Block Diagram

The S5 Engine

The S5620 processor is powered by the Stretch S5 engine, which incorporates the widely accepted Tensilica® Xtensa® RISC processor core and the powerful Stretch Instruction Set Extension Fabric (ISEF). The ISEF is a software-configurable data path based on proprietary programmable logic. Using the ISEF, system designers extend the processor instruction set and define the new instructions using only their C/C++ code. As a result, developers get the performance of logic with C/C++ development simplicity—achieving unprecedented performance, easy and rapid development, and significant cost savings. Stretch's S5 engine unlocks the following two major RISC bottlenecks to provide an unparalleled level of performance:

- **Granularity of computations:** Unlike typical RISC processors' ALUs that perform low level operations such as shift, add, and multiply, the ISEF can execute thousands of operations as a single instruction.
- **Data and compute bandwidth:** The S5 uses 32 128-bit wide registers coupled with 128-bit wide access to memory to feed data to the ISEF at a bandwidth not available on any other processors.

Package

- 1053 FCBGA – 35mm x 35mm

Stretch Advantages

How This is Achieved

Design Flexibility

Developers use C/C++ to program the processor and configure the ISEF with custom instructions. Configurability enables application flexibility allowing developers to respond to emerging standards, add new features and support new algorithms with no redesign.

High Compute Performance

“Hot spots” (sequences of operations that are executed many times) are reduced to a single instruction in the ISEF, providing significant performance gains at the same clock rate.

Rapid Development and Faster Time to Market

Product customization by using only C/C++ software simplifies application development and eliminates traditional long development cycles. This software-based approach allows system designers to quickly adapt to changing requirements without changing their hardware.

Lower System Cost

A Stretch processor can replace multiple DSPs or combinations of processors and FPGAs, thereby reducing system and design costs. In addition, the software-only environment eliminates the complexity of hardware/software co-development.

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