



of the MATLAB/Simulink development environment from The MathWorks.

'Ever since IPFlex was founded in 2000, we have maintained an 'applications first' approach, and worked to create an IC development environment that allowed hardware to be described using high-level languages such as C,' said Koichi Hagishima, president and CEO of IPFlex. 'With the release of DAPDNA-FW II IDE ver2.3, we've been able to demonstrate the first step toward that vision.'

An evaluation kit includes the DAPDNA-2 processor and board control libraries, including everything needed for evaluating algorithms using the dynamically reconfigurable processor and creating and testing prototypes. The six



channels of Direct IO provided by the DAPDNA-2 processor are all available via connectors on the board, allowing connection of a wide variety of interface boards for easy system prototyping.

WiMax widens

The latest reconfigurable processor developed by PicoChip (www.picochip.com), the PC102, sampled in June and is finding applications in mobile phone basestations and for the WiMax short range wireless broadband specification. WiMax is still changing in the way it provides a high bandwidth wireless link over a range of a few kilometres to fixed and mobile terminals, so a configurable solution is appropriate, says picoChip.

The PC102 uses 329 processing elements in three varieties for data and control planes,

as well as 15 accelerator blocks for functions such as forward error correction and correlation. This provides up to 197,000MIPS of sustained processing and 38.4GMACs, with 3.3Tbit/sec of interconnect between the different processing elements and 20Gbit/sec of IO. Additional accelerator blocks provide up to 140billion complex-correlation points/sec.

As a demonstration, PicoChip has developed all the software needed for a WiMax modem based around the PC102, to provide a seamless upgrade to the formal 802.16d specification and all different amendments. The same architecture can be upgraded to 802.16e for mobility later this year.

'Our architecture is very well-suited to complex wireless, and delivering a software defined 802.16d system shows this,' said Doug Pulley, co-founder and CTO of picoChip. 'In effect, this is an 802.16 'chipset' for companies who need a system, but with the flexibility a conventional chipset can never support.'

RAP integration

Elixent's (www.elixent.com) Reconfigurable Algorithm Processor (RAP) array of 4bit processing elements has been integrated into Toshiba's MeP system on a chip platform, running alongside Toshiba's MeP-C2 RISC processor. This is being used in an MP3 player currently but is equally suited to MPEG4 and digital TV applications, says Toshiba.

UK chip designer Aspex Semiconductor (www.aspexsemiconductor.com) has also emerged with its LineDancer family of reconfigurable processors. This combines a Sparc core with an array of 4096 PEs that are individually fed by a matrix of interconnect. The chip uses a hierarchy of memories to configure the array and like the DAP/DNA can be configured in a single cycle.

The architecture is optimised for accelerating core video algorithms rather than the whole system, and comes with a software development environment called Activate, based on industry-standard GNU tools.

Companies like Imagineer Systems (www.imagineersystems.com) are using the chip to increase performance of its new texture replacement software called 'monet' for broadcast, film and video post-production.

It uses Aspex's Accelera plug-in PCI card with two Linedancer chips and the Activate tools for accelerating algorithms, giving an increase in performance of 10 to 20 times in the tracking algorithm it uses.

LineDancer is now on 130nm process at Philips Semiconductor and provides 300MHz performance. The company has a high definition version under development.

By NICK FLAHERTY